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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of)
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Ichiro TAKAYAMA et al.)
)
Serial No.: 09/394,345)
)
Filed: September 13, 1999)
)
For: ACTIVE MATRIX TYPE FLAT-PANEL DISPLAY DEVICE)

Group Art Unit: 2778

Examiner: Osorio, R.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents and Trademarks, Washington, D.C. 20231, on

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CLAIM FOR PRIORITY UNDER 35 U.S.C. § 119

Commissioner for Patents
Washington, D. C. 20231

Sir:

The benefit of the following date of the following prior foreign application filed in the following foreign country is hereby requested for the above-identified patent application and priority provided in 35 U.S.C. § 119 is hereby is hereby claimed.

In support of this claim a Certified Copy and a verified English translation of Japanese Patent Application No. 6-267242 are filed herewith.

It is requested that the file of this application be marked to indicate that the requirements of 35 U.S.C. § 119 have been fulfilled and that the U.S. Patent and Trademark Office kindly acknowledge receipt of these documents.

Respectfully submitted,

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Docket No. 0756-2028

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Ichiro TAKAYAMA et al.)
Serial No. 09/394,345) Group Art Unit: 2775
Filed: July 14, 1996) Examiner: OSORIO, R
For: ACTIVE MATRIX TYPE)
FLAT-PANEL DISPLAY DEVICE)

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

I, Ikuko Noda, 3-G, 1551, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages; and

that to the best of my knowledge and belief the following is a true and correct translation of the Japanese Patent Application No. 6-267242 filed on October 31, 1994.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 21st day of August, 2000

Ikuko Noda

Name: Ikuko Noda

[Name of Document] Patent Application
[Reference Number] XR99P242
[Filing Date] October 31, 1994
[Attention] Commissioner, Patent Office
[International Patent Classification] H05B 33/08
[Title of Invention] ELECTROLUMINESCENT DISPLAY DEVICE
[Number of Claims] 2

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[Name of Document] Specification

[Title of the Invention] ELECTROLUMINESCENT DISPLAY DEVICE

[Claims]

1. An electroluminescent display device comprising:

a plurality of electroluminescent (EL) elements;

driver circuits for driving said EL elements; and

redundant circuits incorporated in said driver circuits and acting as backup circuits.

2. An electroluminescent display device comprising:

electroluminescent (EL) elements positioned at individual pixels;

a plurality of thin-film transistor driver circuits for driving said EL elements; and

a selector switch for selecting one of said plural thin-film transistor driver circuits;

and wherein a modulated image data signal is supplied to any one of the thin-film transistor driver circuits to supply an image data signal to the EL elements, for driving the EL elements.

[Detailed Description of the Invention]

[0001]

[Industrial Field of Application]

The present invention relates to an electroluminescent (referred to hereinafter as EL) display device for driving EL elements by using thin-film transistors (referred to hereinafter as TFTs).

[0002]

The display screen of an EL display is made up of a very large number of pixels, e.g., 800 × 480 dots. Therefore, defects occur in TFT driver circuits for driving the EL elements, thus deteriorating the manufacturing yields for EL displays. Therefore, there is a demand for improvement of yields for EL display devices.

[0003]

[Prior Art]

Figs. 4-6 show a conventional example. The conventional example is hereinafter described with reference to the figures.

[0004]

Fig. 4(a) is a block diagram of a panel. This display panel, 10, is provided with a display screen 11, an X-axis shift register 12, and a Y-axis shift register 13.

[0005]

EL power is supplied to the display screen 11 and shift register power is supplied and an X-axis synchronizing signal is inputted to the X-axis shift register 12. Further, shift register power is supplied and a Y-axis synchronizing signal is inputted to the Y-axis shift register 13. The X-axis shift register 12 has an output portion from which an image data signal is output.

[0006]

Fig. 4(b) is an enlarged view of portion A of Fig. 4(a). Each one pixel on the display screen 11 (indicated by a dotted square) is made up of two transistors, one capacitor, and one EL element.

[0007]

The emission operation of this one pixel is as follows. For example, when a select signal y1 is outputted at the Y-axis shift register 13 and a select signal x1 is outputted at the X-axis shift register 12, transistors Ty11 and Tx1 are turned on.

[0008]

Therefore, the image data signal -VL is applied to the gate of a drive transistor M11. Consequently, a current corresponding to the gate voltage flows from the EL power supply to across the drain and source of the drive transistor M11, thus exciting an EL element EL11 into emission.

[0009]

At the next timing, the X-axis shift register 12 turns off the select signal x1. It follows that a select signal x2 is delivered. Since the gate voltage of the drive transistor M11 is retained by a capacitor C11, the emission of the EL element EL11 is sustained until this pixel is selected next.

[0010]

Fig. 5 is a diagram illustrating a conventional X-axis shift register. In Fig. 5, NAND circuits 21 and 22 are wave-shaping circuits to which clock -CL of opposite phase and a low-level (L) start pulse -SP (X-axis synchronizing signal) are respectively applied. Clocked inverters 26-32 and inverters 33-37 are shift registers. Further, inverters 38-43 and NAND circuits 23-25 are logic circuits that output select signals x1-x3, respectively.

[0011]

When one of clock CL and clock -CL of opposite phase is at high level(H), the other assumes a low level (L).

When the applied clock CL is L and the applied clock -CL of opposite phase is H, the clocked inverters become active and operate as inverters. Conversely, when the applied clock CL is H and the clock -CL of opposite phase is L, the clocked inverters assume a high impedance state.

[0012]

For example, the clock CL input and opposite-phase clock -CL input are connected with the clocked inverters 26 and 29 in an opposite relation to each other. Therefore, when the clocked inverter 26 is in an active state, the clocked inverter 29 assumes a high impedance state.

[0013]

Fig. 6 is a diagram illustrating waveforms of the conventional example. The operation of the X-axis shift register shown in Fig. 5 is described with reference to the waveforms of Fig. 6.

(1) The potential at a point A that is the output of a wave-shaping circuit is H when the start pulse -SP (L) is not present. At this time, if the start pulse -SP of L is applied, the point A goes L (see A in Fig. 6).

[0014]

(2) When the point A goes low (L), the clocked inverter 26 becomes active and so a point B becomes high (H). When the clocked inverter 26 assumes a high-impedance state next, the clocked inverter 29 becomes active and, therefore, the state H at the point B is retained during the active period of the clocked inverter 29 (see B in Fig. 6).

[0015]

(3) The waveform at a point C is put out of phase with the waveform at the point B by the inverter 33 (see C in Fig. 6).

(4) The waveform at a point D is delayed by a half clock cycle with respect to the waveform at the point B by the clocked inverter 27 which becomes active simultaneously with the clocked inverter 29 and by a retaining circuit consisting of the inverter 34 and the clocked inverter 30.

[0016]

(5) The waveform at a point E is placed out of phase with the waveform at the point D by the inverter 34 and delayed by a half clock cycle with respect to the waveform at the point C (see E in Fig. 6).

(6) The waveform at a point F is delayed by a half clock cycle with respect to the waveform at the point D by the clocked inverter 28 which becomes active simultaneously with the clocked inverter 30 and by a retaining circuit consisting of the inverter 35 and the clocked inverter 31.

[0017]

(7) The waveform at a point G is placed out of phase with the waveform at the point F by the inverter 35 and delayed by a half clock cycle with respect to the waveform at the point F (see G in Fig. 6).

(8) The signal at a point H is inverted with respect to the signal at the point C by the inverter 38 (see H in Fig. 6). The signal at a point I is inverted with respect to the signal at the point E by the inverter 39 (see I in Fig. 6). The signal at a point J is inverted with respect to the signal at the point G by the inverter 40 (see J in Fig. 6).

[0018]

(9) A point K is the output of the NAND circuit 23. The signals appearing at the points H and E are applied to two inputs of the NAND circuit 23. A point L is the output of

the NAND circuit 24. The signals appearing at the points I and G are applied to two inputs of the NAND circuit 24. A point M is the output of the NAND circuit 25. A signal from the point J and a signal from an inverter (not shown) are applied to two inputs of the NAND circuit 25.

[0019]

(10) The select signal x1 is inverted at the point K by an inverter 41 (see x1 in Fig. 6). This select signal x1 is applied to the gate of the N-channel field-effect transistor Tx1. Therefore, when the select signal x1 goes high (H), the transistor Tx1 turns on, thus conducting current between its drain and source.

[0020]

(11) The select signal x2 is inverted at the point L by the inverter 42 (see x2 in Fig. 6). This select signal x2 is applied to the gate of the N-channel field-effect transistor Tx2. Therefore, when the select signal x2 goes high (H), the transistor Tx2 turns on.

[0021]

(12) The select signal x3 is inverted at the point M by the inverter 43 (see x3 in Fig. 6). This select signal x3 is applied to the gate of the N-channel field-effect transistor Tx3. Therefore, when the select signal x3 goes high (H), the transistor Tx3 turns on.

[0022]

In this way, the select signals x1, x2, x3, and so on are successively shifted by a half clock cycle.

[0023]

[Problem to be Solved by the Invention]

In the above-described conventional structure, if the number of pixels on the EL display screen increases, the possibility of occurrence of defective TFTs increases accordingly. There arises a problem that this deteriorates the yield.

[0024]

The present invention is intended to improve the yield by providing a backup TFT driver circuit and switching the operating circuit from a defective TFT driver circuit to the backup one in order to solve the conventional problem described above.

[0025]

[Means for Solving the Problem]

To solve the foregoing problem, the present invention provides the following structure.

Fig. 1 shows diagrams illustrating one example of the present invention. Fig. 1(a) is a block diagram of a panel. Fig. 1(b) is an enlarged view of portion A of Fig. 1(a).

[0026]

In Fig. 1(a), an EL display panel 10 has a display screen 11, an X-axis shift register

12, and a Y-axis shift register 13. EL power is supplied to the display screen 11. Shift register power is supplied and an X-axis synchronizing signal is inputted to the X-axis shift register 12. Shift register power is supplied and a Y-axis synchronizing signal is inputted to the Y-axis shift register 13. Further, the X-axis shift register 12 has an output portion from which a modulated image data signal is output.

[0027]

In Fig. 1(b), each one pixel (indicated by a dotted square) on the display screen 11 has two drive TFTs M11r and M11l and two drive TFTs M12r and M12l for driving EL elements EL11 and EL12, respectively.

[0028]

When transistors Ty11r and Tx1r that are selector switches are turned on by the select signals y1 and x1r, the drive TFT M11r is driven by the modulated image data signal -VL1. When transistors Ty11l and Tx1l that are selector switches are turned on by the select signals y1 and X1l, the drive TFT M11l is driven by the modulated image data signal -VL1.

[0029]

The drive TFT M12r is driven by the modulated image data signal -VL1 when the transistors Ty12r and Tx1r that are selector switches are turned on by the select signals y2 and x1r. The drive TFT M12l is driven by the modulated image data signal -VL1 when the transistors Ty12l and Tx1l that are selector switches are turned on by the select signals y2 and X1l.

[0030]

Capacitors C11r, C11l, C12r, and C12l retain the voltages for driving the drive TFTs, respectively.

[0031]

[Operation]

The operation of the present invention based on the above-described structure is described.

Two sets of driver circuits are provided to drive one EL element. Usually, any one is used and if one is at fault, the other driver circuit is used.

[0032]

In Fig. 1(b), it is assumed as an example that the drive TFT 11r that drives the EL element EL11 is at fault. When the transistors Ty11r and Tx1r are turned on by the select signals y1 and x1r, an image data signal that is off level (in this case, "H"), i.e., the modulated image data signal -VL1, is supplied to the gate of the drive TFT M11r.

[0033]

When the transistors Ty11l and Tx1l are then turned on by the select signals y1 and x1l, the modulated image data signal -VL1 that is an image data signal is supplied to the gate

of the drive TFT M11l. This modulated image data signal -VL1 is retained by the capacitor C11l.

[0034]

In this way, the conventional X-axis select signal is divided into twice X-axis select signals x1r and x1l corresponding to the former half and the latter half. Using these signals x1r and x1l, the modulated image data signal -VL1 is so produced that each EL element is driven by the former-half select signal per pixel. If a defective drive TFT M11r is selected, the image data signal is not supplied but supplied when the drive TFT M11l is selected. In this way, the EL element EL11 is driven by the drive TFT M11l that is normal.

[0035]

As described above, a backup redundant circuit is provided for TFT driver circuits per pixel. If any one of the TFT driver circuits is at fault, the operating circuit can be switched to the backup circuit. Hence, the yield can be improved.

[0036]

[Embodiment]

Examples of the present invention are hereinafter described with reference to the drawings.

Figs. 1-3 show diagrams illustrating embodiments of the present invention. Note that like components are indicated by like reference numerals throughout various figures including Figs. 4-6.

[0037]

Fig. 1 illustrates one example of the present invention. Fig. 1(a) is a block diagram of a panel. Fig. 1(b) is an enlarged view of portion A of Fig. 1(a).

In Fig. 1(a), an EL display panel 10 has a display screen 11, an X-axis shift register 12, and a Y-axis shift register 13. EL power is supplied to the display screen 11. Shift register power is supplied and an X-axis synchronizing signal is inputted to the X-axis shift register 12. Shift register power is supplied and a Y-axis synchronizing signal is inputted to the Y-axis shift register 13. Further, the X-axis shift register 12 has an output portion from which an image data signal is output.

[0038]

In Fig. 1(b), each one pixel (indicated by a dotted square) on the display screen 11 has two drive TFTs M11r and M11l and two drive TFTs M12r and M12l for driving EL elements EL11 and EL12, respectively, which are made of an organic EL film.

[0039]

The drive TFT M11r is driven by the modulated image data signal -VL1 when the transistors Ty11r and Tx1r that are selector switches are turned on by select signals y1 and x1r. The drive TFT M11l is driven by the modulated image data signal -VL1 when the transistors

Ty11l and Tx1l that are selector switches are turned on by the select signals y1 and x1l.

[0040]

The drive TFT M12r is driven by the modulated image data signal -VL1 when the transistors Ty12r and Tx1r that are selector signals are turned on by the select signals y2 and x1r. The drive TFT M12l is driven by the modulated image data signal -VL1 when the transistors Ty12l and Tx1l that are selector switches are turned on by the select signals y2 and x1l.

[0041]

Capacitors C11r, C11l, C12r, and C12l retain the voltages for driving the drive TFTs, respectively.

The select signals y1 and y2 outputted from the Y-axis shift register 13 are the same as conventional ones shown in Fig. 4(b). However, the select signals x1r and x1l outputted from the X-axis shift register 13 are pulses that are twice as many as pulses produced by the conventional example described above. The image data signal results in the modulated image data signal -VL1 synchronized with the select signal x1r or x1l.

[0042]

Fig. 2 is a diagram illustrating driver circuits for one pixel and the modulated image data signal. Fig. 2(a) illustrates the EL element driver circuit for one pixel, the driver circuit being shown in Fig. 1(b).

In Fig. 2(a), there are provided two P-channel drive TFTs Mnmr and Mnml connected with the EL power supply 1 and an EL element ELnm driven by the drive TFT Mnmr or Mnml.

[0043]

A series circuit of N-channel field-effect transistors Tynmr and Txnr that are selector switches are connected with the gate of this drive TFT Mnmr. A series circuit of N-channel field-effect transistors Tynml and Txnl that are selector switches are connected with the gate of the drive TFT Mnml.

[0044]

The operation of the EL element driver circuit shown in Fig. 2(a) is as follows. When the select signal ym for the Y-axis shift register 13 is H, if the select signal xnr for the X-axis shift register 12 goes high (H), the transistors Tynmr and Txnr that are select switches are turned on. Therefore, the resulting modulated image data signal -VL1 is supplied to the gate of the drive TFT Mnmr. A current corresponding to this gate voltage is supplied to the EL element ELnm from the EL power supply 1. When the selector switches are turned off, the gate voltage is retained in the capacitor Cnmr. In this way, EL element emits light according to the current.

[0045]

When the select signal ym is H, if the select signal xnl goes high (H), the transistors Tynml and Txnl that are selector switches are turned on. Therefore, the resulting modulated image data signal -VL1 is supplied to the gate of the drive TFT Mnml. The image data signal is retained in the capacitor Cnmr by the select signal xnr. At this time, the image data signal gives the modulated image data signal -VL at off level.(In this case, the image data signal is H.)

[0046]

Fig. 2(b) is a block diagram of a generating circuit of the modulated image data signal. In Fig. 2(b), a phase selector circuit 2 divides the output interval of the image data signal -VL which is synchronized to the conventional shift registers x1-x3, into a former half and a latter half. (One pixel is selected during this output interval.) If information from a ROM 3 does not contain any information about a defective TFT, the image data is outputted only during the former half of the interval, for example, (while the latter half is blanked off). If the information from the ROM 3 contains information about a defective TFT, the image data is outputted only during the latter half of the interval; (the former half is blanked off). In this way, the modulated image data signal -VL is delivered.

[0047]

The ROM 3 is a read-only memory memorizing that which of the TFTs is defective at product inspection. A signal indicating a defective TFT is produced at the instant when a pixel containing a defective TFT is selected.

[0048]

Fig. 3 is a timing chart of the example. Fig. 3(a) indicates a timing chart of a conventional example used for comparison. Fig. 3(b) indicates a timing chart of an example of the present invention.

[0049]

In Fig. 3(a), image data signal -VL varies in response to shift pulses for X-axis select signals xn, xn + 1, xn + 2, xn + 3, xn + 4, xn + 5, and so forth.

[0050]

In Fig. 3(b), with respect to the X-axis select signals, shift pulses for two select signals corresponding to the former half and latter half, respectively, are outputted per pixel, i.e., xnr and xnl, xn + 1r and xn + 1l, xn + 2r and xn + 21, and so forth.

[0051]

The case in which a defective TFT exists during the interval of the select signal xn + 2r, for example, as shown in Fig. 3(b) is described.

The modulated image data signal -VL1 is delivered from the phase selector circuit 3 as follows. Where the pixel contains no defective TFT, when the former-half select signals xnr and xn + 1r are outputted, the image data signal is outputted. Where the pixel contains a

defective TFT, the image data signal is delivered when the latter-half select signal xn + 21 is delivered.

[0052]

In the example described above, two drive circuits for driving TFTs are provided in one pixel. Three or more drive circuits may also be provided. Furthermore, the transistors forming the drive TFTs or selector switches may have different channels.

[0053]

[Effects of the Invention]

As described thus far, the present invention produces the following effects.

(1) In accordance with the invention set forth in claim 1, the yield can be improved because of provision of backup redundant circuits.

[0054]

(2) In accordance with the invention set forth in claim 2, since an image data signal is supplied to any one of plural drive TFTs within one pixel to select a driver circuit, the operating circuit can be easily switched to the backup drive circuit.

[Brief Description of Drawings]

[Fig. 1] is a diagram illustrating one example of the present invention. [Fig. 2] is a diagram illustrating driver circuits for one pixel and the modulated image data signal according to the present embodiment.

[Fig. 3] is a timing chart of the present embodiment.

[Fig. 4] is a diagram illustrating the conventional example.

[Fig. 5] is a diagram illustrating a conventional X-axis shift register

[Fig. 6] is a diagram illustrating waveforms of the conventional example.

[Explanation of Marks]

10	display panel
11	display screen
12	X-axis shift register
13	Y-axis shift register
C11r, C11l, C12r, C12l	capacitor
EL11, EL12	EL element
M11r, M11l, M12r, M12l	drive TFT
Ty11r, Ty11l, Ty12r, Ty12l, Tx1r, Tx11	transistor(selection switch)
x1r, x11	select signal (X-axis)
y1,y2	select signal (Y-axis)
-VL1	module image data signal

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２０００年 ８月 ４日

特許庁長官
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